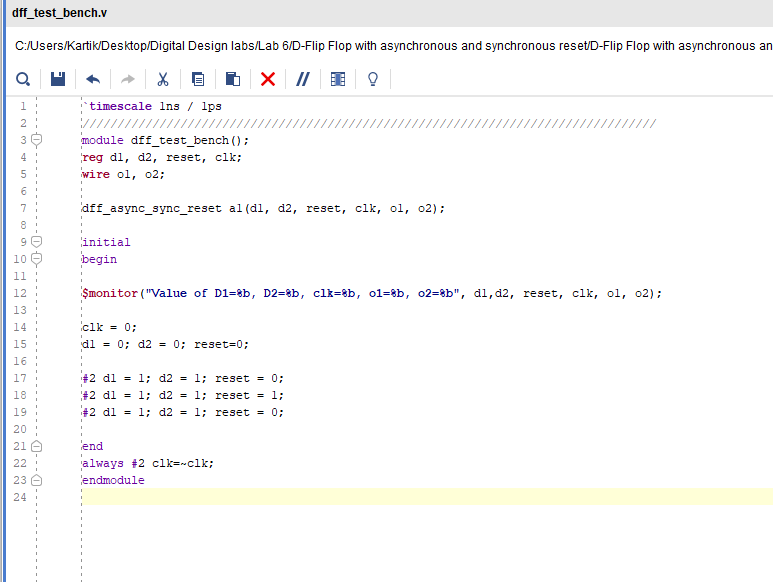
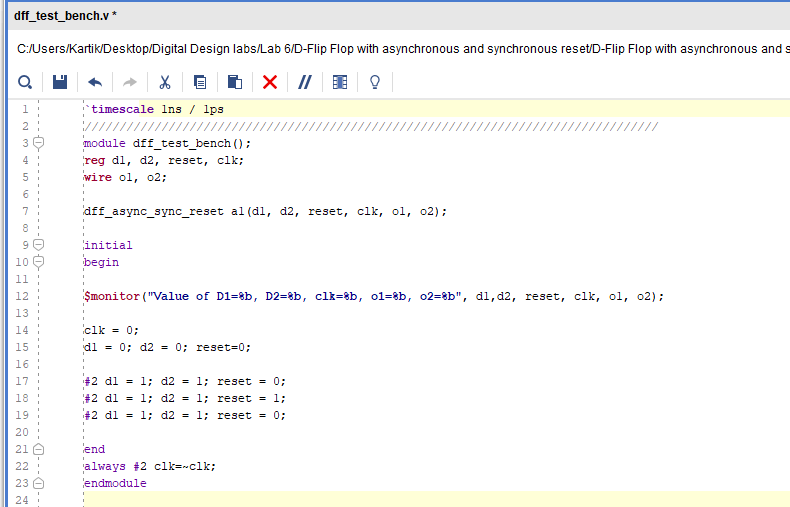
**(EEL2020)** **DIGITAL DESIGN LAB6 REPORT**

KARTIK CHOUDHARY B20CS025

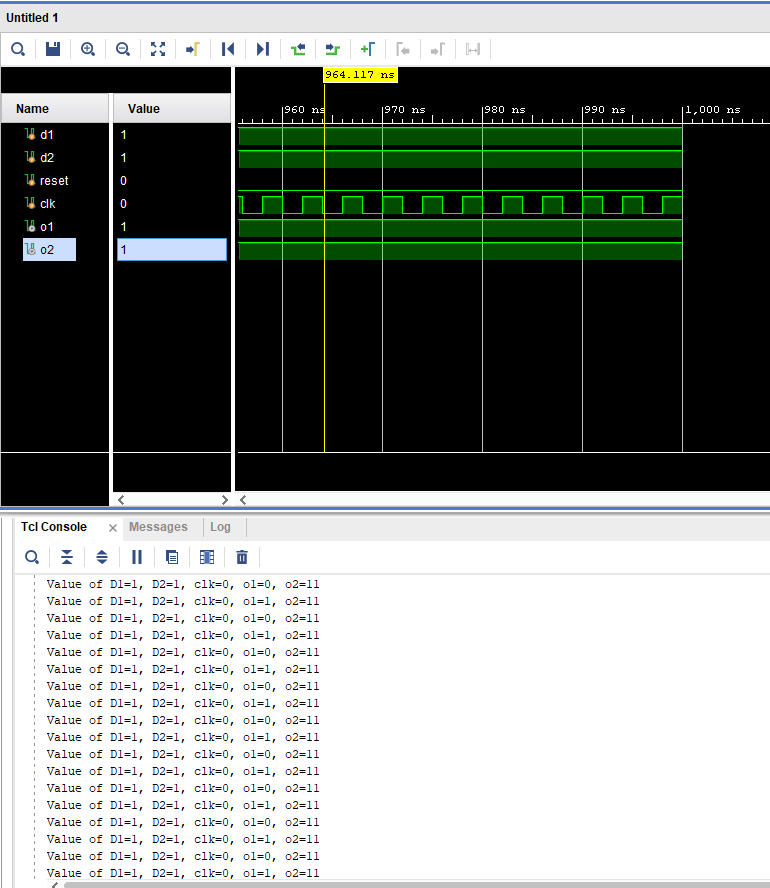
**Work** 1. Write a program to implement a D f/f with synchronous and asynchronous reset. *Test bench*

**

*Verilog Code*

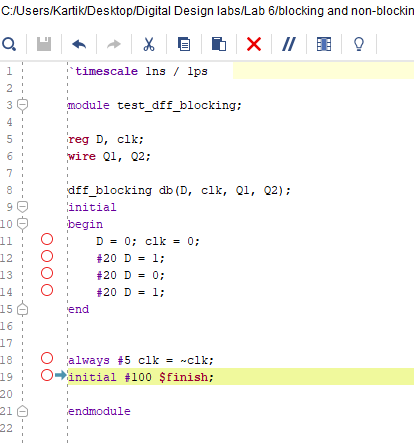
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*Waveform*

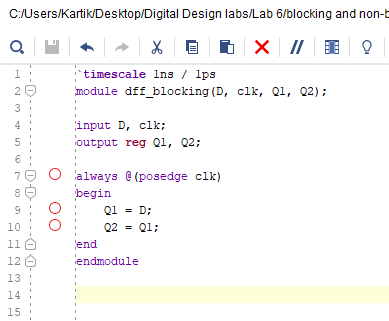


**Work 2:** Test the operation of blocking and non-blocking assignments using two D flip flops.

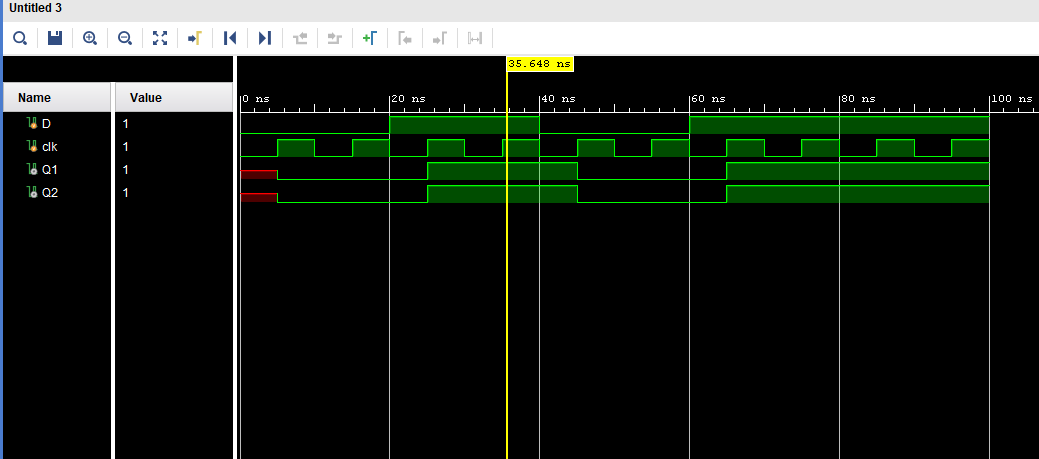
*Test Bench for blocking assignment*

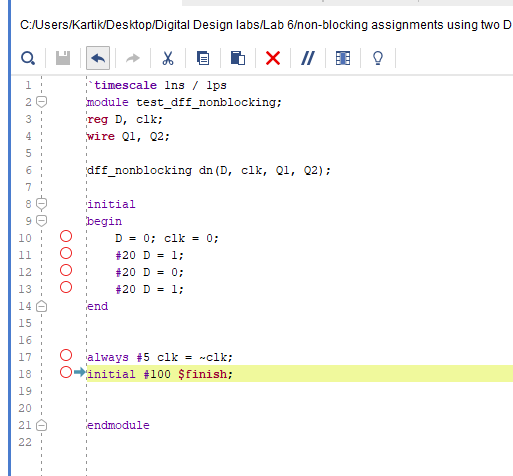
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*Verilog Code for blocking assignment*

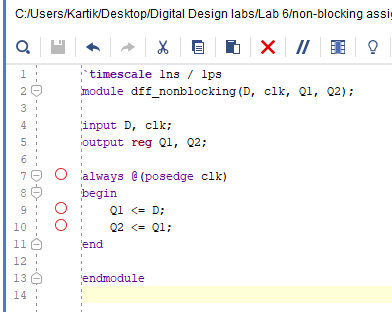
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*Waveform for blocking assignment*

**

*Test Bench for Non-blocking assignment* **

*Verilog Code for Non-blocking assignment*

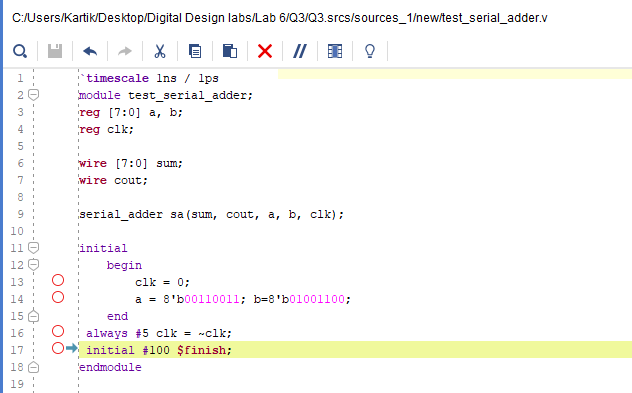
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*Waveform for Non-blocking assignment*

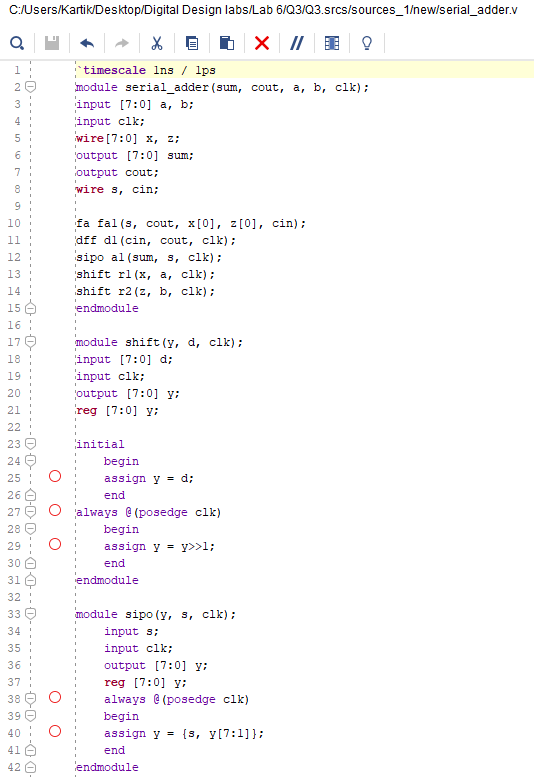
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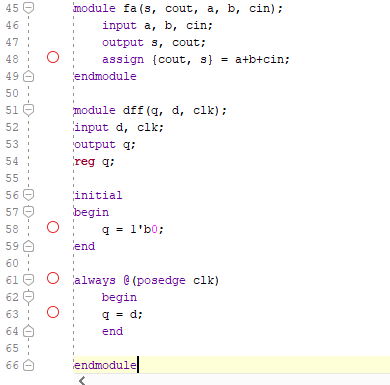
**3.** Implement the 8-bit serial addition (A+B) operation using shift register and a Full Adder. Load the two registers from input using parallel loading. The result should be stored in register A. Find the number of clocks cycles your design would take to implement the complete operation.

*Test Bench*

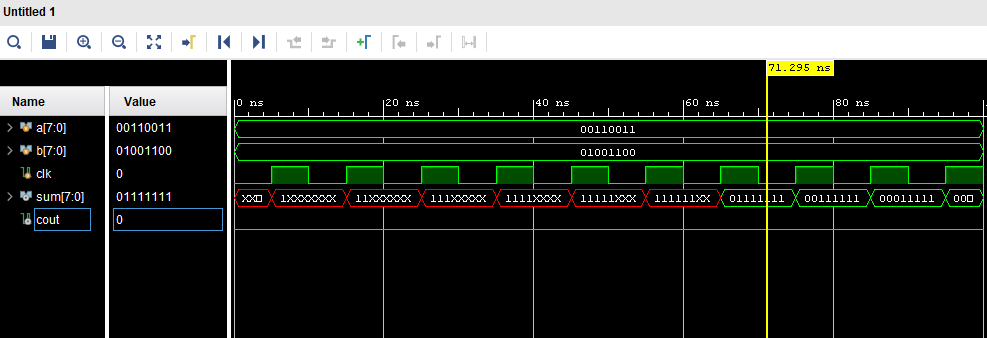


*Verilog Code*

**

**

*Waveform*

**